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EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,454	SWEET, JIM	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-17,19-24 and 27-33* is/are rejected.

7)☒ Claim(s) *9,10,18,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 33 have been examined.

Response to Arguments

Regarding applicant's argument that there would be no motivation to combine Davis et al. with Baker et al., Examiner cites that the invention of Davis et al. pertains to the field of accessing memory by processors (paragraph 7). Similarly, the invention of Baker et al. pertains to accessing memory by processors (column 1, lines 9 – 16). One of ordinary skill in this art seeking to reduce the cost of, and improve the reliability of the system of Davis et al. would look to the invention of Baker et al. as a means of doing so. Therefore, Examiner cannot allow claims 1, 2, 11, and 12.

Regarding applicant's argument that there would be no motivation to combine Davis et al., with Baker et al., and also with Ando et al., Examiner cites that the invention of Davis et al. pertains to accessing registers by a processor(s) (paragraphs 18, 23). Similarly, the invention of Ando et al. pertains to accessing registers by a processor (column 1, lines 15 – 24). One of ordinary skill in this art seeking to reduce the cost of the system of Davis et al. (by simplifying and thereby reducing the size of the decoding circuit; column 7, lines 9 – 24) would look to the invention of Ando et al. as a means of doing so. Therefore, Examiner cannot allow claims 13 – 15.

Response to Applicant's arguments pertaining to claims 19, 20, 27, 28, and 29 – 33 follows similar rationale as stated above.

Applicant's arguments with respect to claims 3, 5, 6, 8 – 10, 16 – 18, and 20 – 26 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Figure 2B, item 205 as disclosed in paragraph 35. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al.

With regard to claim 1, Davis et al. teach a method for sharing hardware resources in a digital system, the method comprising:

Determining whether a hardware resource (paragraph 21 describes a semaphore being mapped to a memory, data store, embedded processor) is in use by monitoring contents of at least one of a plurality of semaphore registers (Figure 4 shows the process of a thread attempting to lock a resource. In the case where the thread wins arbitration, but finds the semaphore already locked, it may return back to the round robin selection (start, item 100, item 110, item 120, item 130, item 150, item 170). Examiner interprets this as the thread monitoring the contents of semaphore registers "Sem_Val" and "Sem_Lock").

Davis et al. fail to teach accessing said monitored contents of said pluralit y of semaphore registers by using a limited-width test bus whose bus width contains less than a number of bits needed to individually address each of said plurality of semaphore registers.

Baker et al. teach a limited-width test bus whose bus width contains less than a number of bits needed to individually address all of the address space (column 2, lines 59 – 63).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the limited-width test bus as taught by Baker et al. into the method of Davis et al. for the purpose of reducing the number of pins needed for the bus. This would have been obvious since Baker et al. teach that reducing the number of pins required for the bus would reduce the cost of the system and increase the reliability (column 1, lines 23 – 45).

With regard to claim 2, Baker et al. teach the additional limitation of assigning a portion of said limited-width test bus to address each of said plurality of semaphore registers (where a semaphore register may be interpreted as a memory device; column 3, lines 11 – 14, 24 – 27) and assigning a remaining portion of said limited-width test bus to address each register bit location in said plurality of semaphore registers (column 3, lines 11 – 14, 43 – 47).

With regard to claim 11, Davis et al. teach the additional limitation of a method according to claim 1 further comprising determining from said monitored contents of said plurality of semaphore registers an identifier of a software thread using said hardware resource (paragraph 25).

With regard to claim 12, Davis et al. teach the additional limitation of a method according to claim 11, further comprising tracking said software thread that is using said hardware resource (paragraph 25; Examiner interprets storing the thread identifier in a semaphore register as tracking the software thread, i.e., maintaining knowledge of what hardware resources it is using).

* * *

Claims 13 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Ando et al.

With regard to claim 13, Davis et al. teach a plurality of semaphore registers (paragraph 25; Figure 3), but fail to teach arranging the registers into register blocks, and selecting one of said plurality of semaphore register blocks to be accessed by a limited-width test bus.

Baker et al. teach a limited-width test bus ((column 2, lines 59 – 63).

Ando et al. teach arranging a plurality of registers into register blocks (Figure 1, items 20_1 to 20_4), and selecting one of said plurality of registers to be accessed by a bus (bus: Figure 1, item 1; selection: column 4, lines 9 – 12, 17 – 26; column 6, lines 6 – 9, 17 – 20)

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the limited-width test bus as taught by Baker et al. into the method of Davis et al. for the purpose of reducing the number of pins needed

for the bus. This would have been obvious since Baker et al. teach that reducing the number of pins required for the bus would reduce the cost of the system and increase the reliability (column 1, lines 23 – 45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to organize the semaphore registers as taught by Davis et al. into register blocks as taught by Ando et al. This would have been obvious in order to simplify the decoding circuit and reduce the number of signal lines required to access the registers (column 7, lines 9 – 24).

With regard to claim 14, Baker et al. teach the additional limitation of assigning at least one bit line in the bus to select one of said plurality of semaphore register blocks (where a memory device may be interpreted as a register block; column 3, lines 24 – 27).

With regard to claim 15, Baker et al. teach the additional limitation of assigning a portion of said limited-width test bus to address each of said plurality of semaphore registers (where a semaphore register may be interpreted as a memory device; column 3, lines 11 – 14, 24 – 27) and assigning a remaining portion of said limited-width test bus to address each register bit location in said plurality of semaphore registers (column 3, lines 11 – 14, 43 – 47).

* * *

Claims 19, 20, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al.

With regard to claim 19, Davis et al. teach a system for sharing hardware resources in a digital system, the system comprising:

A plurality of hardware resources (paragraph 21 describes a semaphore being mapped to a memory, data store, embedded processor – Examiner interprets these as hardware resources);

A plurality of semaphore registers coupled to said plurality of hardware resources (paragraph 21 describes a semaphore being mapped to a memory, data store, embedded processor);

Davis et al. fail to teach a limited-width test bus coupled to said plurality of semaphore registers, wherein said limited-width test bus contains less than a number of bits needed to individually address each of said plurality of semaphore registers.

Baker et al. teach a limited-width test bus whose bus width contains less than a number of bits needed to individually address all of the address space (column 2, lines 59 – 63).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the limited-width test bus as taught by Baker et al. into the method of Davis et al. for the purpose of reducing the number of pins needed for the bus. This would have been obvious since Baker et al. teach that reducing the

number of pins required for the bus would reduce the cost of the system and increase the reliability (column 1, lines 23 – 45).

With regard to claim 20, Baker et al. teach the additional limitation of assigning a portion of said limited-width test bus to address each of said plurality of semaphore registers (where a semaphore register may be interpreted as a memory device; column 3, lines 11 – 14, 24 – 27) and assigning a remaining portion of said limited-width test bus to address each register bit location in said plurality of semaphore registers (column 3, lines 11 – 14, 43 – 47).

With regard to claim 27, Davis et al. teach the additional limitation of a system according to claim 19, wherein a processor coupled to said limited-width test bus (where a processor may be interpreted as a semaphore coprocessor; paragraph 18) determines an identifier of a software thread that is using one of said hardware resources based on contents of at least one of said plurality of semaphore registers (where an identifier may be interpreted as a thread ID; paragraph 25).

With regard to claim 28, Davis et al. teach the additional limitation of a method according to claim 27, wherein said processor tracks said software thread that is using said hardware resource (paragraph 25; Examiner interprets storing the thread identifier in a semaphore register as tracking the software thread, i.e., maintaining knowledge of what hardware resources it is using).

* * *

Claims 29 – 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Ando et al.

With regard to claim 29, Davis et al. teach a plurality of semaphore registers, but fail to teach the registers organized in blocks, a selector coupled to said plurality of semaphore register blocks, and a limited-width test bus connected to said plurality of semaphore registers blocks of said selector.

Ando et al. teach a plurality of register blocks comprising a plurality of registers (Figure 1, items 20_1 to 20_4), and a selector coupled to said plurality of semaphore register blocks (where a selector may be interpreted as a decoder; Figure 1, item 27; column 4, lines 9 – 12, 17 – 26; column 6, lines 6 – 9, 17 – 20).

Baker et al. teach a limited-width test bus (column 2, lines 59 – 63).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to organize the semaphore registers as taught by Davis et al. into register blocks as taught by Ando et al. This would have been obvious in order to simplify the decoding circuit and reduce the number of signal lines required to access the registers (column 7, lines 9 – 24).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the limited-width test bus as taught by Baker et al. into the method of Davis et al. for the purpose of reducing the number of pins needed

for the bus. This would have been obvious since Baker et al. teach that reducing the number of pins required for the bus would reduce the cost of the system and increase the reliability (column 1, lines 23 – 45).

With regard to claim 30, Baker et al. teach the additional limitation of assigning at least one bit line in the bus to select one of said plurality of semaphore register blocks (where a memory device may be interpreted as a register block; column 3, lines 24 – 27).

With regard to claim 31, Davis et al. teach the additional limitation wherein a processor (where a processor may be interpreted as a semaphore coprocessor; paragraph 18) determines whether a hardware resource is in use in said selected one of said plurality of semaphore register blocks (paragraphs 23, 25).

With regard to claim 32, Davis et al. teach the additional limitation of a system further comprising determining from said monitored contents of said plurality of semaphore registers an identifier of a software thread using said hardware resource (paragraph 25).

With regard to claim 33, Davis et al. teach the additional limitation of a system, further comprising tracking said software thread that is using said hardware resource (paragraph 25; Examiner interprets storing the thread identifier in a semaphore register

as tracking the software thread, i.e., maintaining knowledge of what hardware resources it is using).

* * *

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Flynn et al.

Regarding claim 3, Davis et al., and Baker et al., fail to teach where said determination of whether said hardware resource is in use further comprises ORing each register bit location in each of said plurality of semaphore registers if a protocol reset state is logic 0.

Flynn et al. teach determination of whether a hardware resource is in use comprises ANDing each register bit location (Figure 6; column 15, line 57 – column 16, line 5; in each of said plurality of semaphore registers (Examiner interprets the resources available vector as a plurality of semaphore registers since each vector contains bits in registers which mark whether or not a resource is being used; column 7, lines 47 – 53; column 14, line 55 – column 15, line 7) if a protocol reset state is logic 0 (where a protocol reset state is interpreted as a logic state of the semaphore register value; Examiner notes that this determination is made regardless of the logic states of the register values, and therefore meets this limitation).

Flynn et al. fail to explicitly teach ORing, however, Balch teaches that OR and AND gates are readily interchangeable by using inverters (e.g., a NOT gate) through the

use of DeMorgan's Law (page 8). DeMorgan's law is old and well known in this art, and therefore, Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to apply it to use OR gates with inverting gates and achieve the same functionality as with using the AND gates of Flynn et al. Additionally, Flynn et al. hints that other implementations would be apparent to those skilled in the art (column 16, lines 59 – 66).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the method of Flynn et al. with the method of Davis et al. and Baker et al. for the purpose of providing a means of arbitrating access to shared resources. This would have been obvious since Flynn et al. teach that their method makes efficient use of all system resources at the time they are available, and guarantees requests for resources to be honored within a reasonable time so that a requesting unit is never locked out (column 3, line 58 – column 4, line 3; column 18, lines 46 – 48, 56 – 59).

Regarding claim 4, Flynn et al. fails to explicitly teach the limitation where if a result of said determination logic is logic 1, then said hardware resource is in use; and if result of said determination is logic 0, then said hardware resource is not in use. Rather, Flynn et al. teach when the result of determination is logic 1, then said hardware resource is not in use, and if result of said determination is logic 0, then said hardware resource is in use (column 15, line 66 – column 16, line 5). Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of

invention by applicant to invert the output of the determination logic of Flynn et al. to achieve this result by using an inverter (e.g., a NOT gate).

Regarding claim 5, Flynn et al. teach the additional limitation further comprising addressing each one of said plurality of semaphore registers by coupling at least one OR gate utilized for said ORing to a bit line in said limited-width test bus (Figure 6, item 172 shows a bit line coupled to AND gate 172; As discussed in the rejection of claim 3, AND gates may be implemented from OR gates, and therefore meets this limitation. Examiner broadly interprets a limited width test bus as a bus of fixed width.).

* * *

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Flynn et al.

Regarding claim 6, Davis et al., and Baker et al., fail to teach where said determination of whether said hardware resource is in use further comprises ANDing each register bit location in each of said plurality of semaphore registers if a protocol reset state is logic 1.

Flynn et al. teach determination of whether a hardware resource is in use comprises ANDing each register bit location (Figure 6; column 15, line 57 – column 16, line 5; in each of said plurality of semaphore registers (Examiner interprets the resources available vector as a plurality of semaphore registers since each vector

contains bits in registers which mark whether or not a resource is being used; column 7, lines 47 – 53; column 14, line 55 – column 15, line 7) if a protocol reset state is logic 0 (where a protocol reset state is interpreted as a logic state of the semaphore register value; Examiner notes that this determination is made regardless of the logic states of the register values, and therefore meets this limitation).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the method of Flynn et al. with the method of Davis et al. and Baker et al. for the purpose of providing a means of arbitrating access to shared resources. This would have been obvious since Flynn et al. teach that their method makes efficient use of all system resources at the time they are available, and guarantees requests for resources to be honored within a reasonable time so that a requesting unit is never locked out (column 3, line 58 – column 4, line 3; column 18, lines 46 – 48, 56 – 59).

Regarding claim 7, Flynn et al. teach the additional limitation where if the result of determination is logic 1, then said hardware resource is not in use, and if result of said determination is logic 0, then said hardware resource is in use (column 15, line 66 – column 16, line 5). Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to invert the output of the determination logic of Flynn et al. to achieve this result by using an inverter (e.g., a NOT gate).

Regarding claim 8, Flynn et al. teach the additional limitation further comprising addressing each one of said plurality of semaphore registers by coupling at least one AND gate utilized for said ANDing to a bit line in said limited-width test bus (Figure 6, item 172 shows a bit line coupled to AND gate 172; Examiner broadly interprets a limited width test bus as a bus of fixed width.).

* * *

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Flynn et al.

Regarding claim 16, Davis et al., and Baker et al., fail to teach where said determination of whether said hardware resource is in use further comprises ORing each register bit location in each of said plurality of semaphore registers if a protocol reset state is logic 0.

Flynn et al. teach determination of whether a hardware resource is in use comprises ANDing each register bit location (Figure 6; column 15, line 57 – column 16, line 5; in each of said plurality of semaphore registers (Examiner interprets the resources available vector as a plurality of semaphore registers since each vector contains bits in registers which mark whether or not a resource is being used; column 7, lines 47 – 53; column 14, line 55 – column 15, line 7) if a protocol reset state is logic 0 (where a protocol reset state is interpreted as a logic state of the semaphore register

value; Examiner notes that this determination is made regardless of the logic states of the register values, and therefore meets this limitation).

Flynn et al. fail to explicitly teach ORing, however, Balch teaches that OR and AND gates are readily interchangeable by using inverters (e.g., a NOT gate) through the use of DeMorgan's Law (page 8). DeMorgan's law is old and well known in this art, and therefore, Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to apply it to use OR gates with inverting gates and achieve the same functionality as with using the AND gates of Flynn et al. Additionally, Flynn et al. hints that other implementations would be apparent to those skilled in the art (column 16, lines 59 – 66).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the method of Flynn et al. with the method of Davis et al. and Baker et al. for the purpose of providing a means of arbitrating access to shared resources. This would have been obvious since Flynn et al. teach that their method makes efficient use of all system resources at the time they are available, and guarantees requests for resources to be honored within a reasonable time so that a requesting unit is never locked out (column 3, line 58 – column 4, line 3; column 18, lines 46 – 48, 56 – 59).

* * *

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Flynn et al.

Regarding claim 17, Davis et al., and Baker et al., fail to teach where said determination of whether said hardware resource is in use further comprises ANDing each register bit location in each of said plurality of semaphore registers if a protocol reset state is logic 1.

Flynn et al. teach determination of whether a hardware resource is in use comprises ANDing each register bit location (Figure 6; column 15, line 57 – column 16, line 5; in each of said plurality of semaphore registers (Examiner interprets the resources available vector as a plurality of semaphore registers since each vector contains bits in registers which mark whether or not a resource is being used; column 7, lines 47 – 53; column 14, line 55 – column 15, line 7) if a protocol reset state is logic 0 (where a protocol reset state is interpreted as a logic state of the semaphore register value; Examiner notes that this determination is made regardless of the logic states of the register values, and therefore meets this limitation).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the method of Flynn et al. with the method of Davis et al. and Baker et al. for the purpose of providing a means of arbitrating access to shared resources. This would have been obvious since Flynn et al. teach that their method makes efficient use of all system resources at the time they are available, and guarantees requests for resources to be honored within a reasonable time so that a

requesting unit is never locked out (column 3, line 58 – column 4, line 3; column 18, lines 46 – 48, 56 – 59).

* * *

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Flynn et al.

Regarding claim 21, Davis et al., and Baker et al., fail to teach wherein each register bit in each of said plurality of semaphore registers is coupled to an OR gate.

Flynn et al. teach each register bit in each of said plurality of semaphore registers being coupled to an AND gate (Figure 6; column 15, line 57 – column 16, line 5; (Examiner interprets the resources available vector as a plurality of semaphore registers since each vector contains bits in registers which mark whether or not a resource is being used; column 7, lines 47 – 53; column 14, line 55 – column 15, line 7).

Flynn et al. fail to explicitly teach ORing, however, Balch teaches that OR and AND gates are readily interchangeable by using inverters (e.g., a NOT gate) through the use of DeMorgan's Law (page 8). DeMorgan's law is old and well known in this art, and therefore, Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to apply it to use OR gates with inverting gates and achieve the same functionality as with using the AND gates of Flynn et al. Additionally, Flynn et al. hints that other implementations would be apparent to those skilled in the art (column 16, lines 59 – 66).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the method of Flynn et al. with the method of Davis et al. and Baker et al. for the purpose of providing a means of arbitrating access to shared resources. This would have been obvious since Flynn et al. teach that their method makes efficient use of all system resources at the time they are available, and guarantees requests for resources to be honored within a reasonable time so that a requesting unit is never locked out (column 3, line 58 – column 4, line 3; column 18, lines 46 – 48, 56 – 59).

Regarding claim 22, Flynn et al. teach the additional limitation further comprising addressing each one of said plurality of semaphore registers by coupling at least one OR gate utilized for said ORing to a bit line in said limited-width test bus (Figure 6, item 172 shows a bit line coupled to AND gate 172; As discussed in the rejection of claim 3, AND gates may be implemented from OR gates, and therefore meets this limitation. Examiner broadly interprets a limited width test bus as a bus of fixed width.).

* * *

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Flynn et al.

Regarding claim 23, Davis et al., and Baker et al., fail to teach wherein each register bit in each of said plurality of semaphore registers is coupled to an AND gate.

Flynn et al. teach wherein each register bit in each of said plurality of semaphore registers is coupled to an AND gate (Figure 6; column 15, line 57 – column 16, line 5; Examiner interprets the resources available vector as a plurality of semaphore registers since each vector contains bits in registers which mark whether or not a resource is being used; column 7, lines 47 – 53; column 14, line 55 – column 15, line 7).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the method of Flynn et al. with the method of Davis et al. and Baker et al. for the purpose of providing a means of arbitrating access to shared resources. This would have been obvious since Flynn et al. teach that their method makes efficient use of all system resources at the time they are available, and guarantees requests for resources to be honored within a reasonable time so that a requesting unit is never locked out (column 3, line 58 – column 4, line 3; column 18, lines 46 – 48, 56 – 59).

Regarding claim 24, Flynn et al. teach the additional limitation further comprising addressing each one of said plurality of semaphore registers by coupling at least one AND gate utilized for said ANDing to a bit line in said limited-width test bus (Figure 6, item 172 shows a bit line coupled to AND gate 172; Examiner broadly interprets a limited width test bus as a bus of fixed width.).

Allowable Subject Matter

Claims 9, 10, 18, 25, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither teaches nor suggests all of the claimed subject matter of claims 9, 18, and 25 including **"XORing corresponding register bit locations in each one of said plurality of semaphore registers," "determining a software thread identifier by XORing corresponding register bit locations in each one of said plurality of semaphore registers," "corresponding register bit locations in each one of said plurality of semaphore registers are coupled to an XOR gate."** Claims 10 and 26 are allowable based upon their dependence to claims 9 and 25.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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